(12) UK Patent Application (19) GB (11) 2 373 974 (13) A

(43) Date of A Publication 02.10.2002

(21) Application No 0200033.9

(22) Date of Filing 02.01.2002

(30) Priority Data
(31) 09754667 (32) 04.01.2001 (33) US

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(51) INT CL[7]
H04L 25/08 , H03K 19/003 // H03K 19/0185

(52) UK CL (Edition T)
H4P PPC
H3P PHFD
H3T T2B3 T2T3F T3V T4D

(56) Documents Cited
GB 2368475 A US 6127839 A
US 5304856 A

(58) Field of Search
UK CL (Edition T) H3P PDM PHFD PHFN PHX , H4P PPC
INT CL[7] G06F 13/40 , H03K 19/003 19/0175 19/018 19/0185 , H04L 25/02 25/08

(54) Abstract Title
An adjustable terminating resistance and matching current shunt

(57) Variation in the termination potential Vterm is reduced by a shunt current network 120-134 which sinks current from the Vterm supply when the bus node PAD is high. When the node PAD is low, current is drawn through the terminating impedance 110-114. The turn-on and turn-off rates for the shunt 120-124 are matched to the current ramps through the terminating impedance 110-114 so that the net current drawn from the termination voltage supply is less data dependent. The termination impedance 110-114 and the shunt impedance 120-124 are programmable to overcome PVT (process, voltage, and temperature) variation.

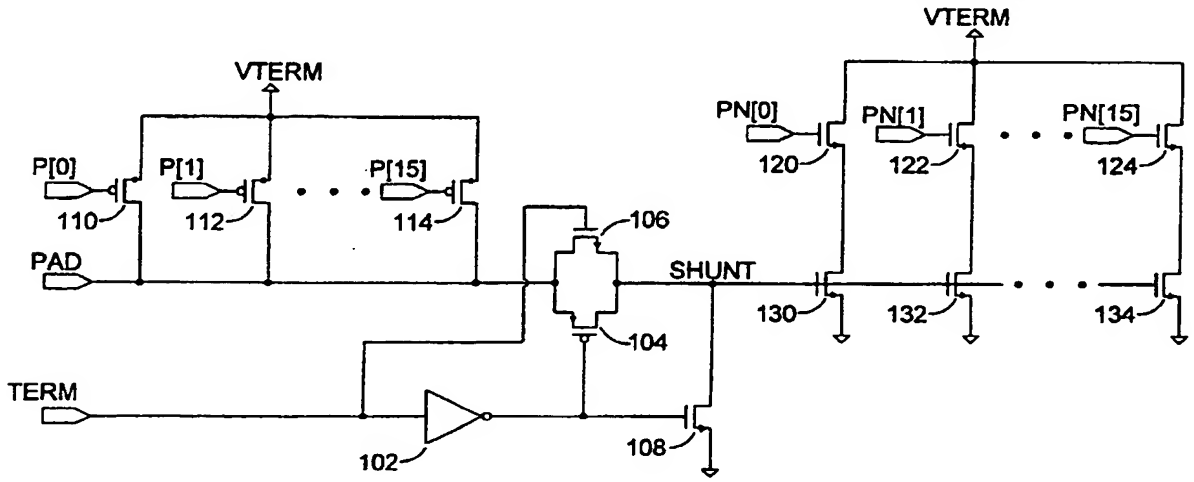

FIG. 1

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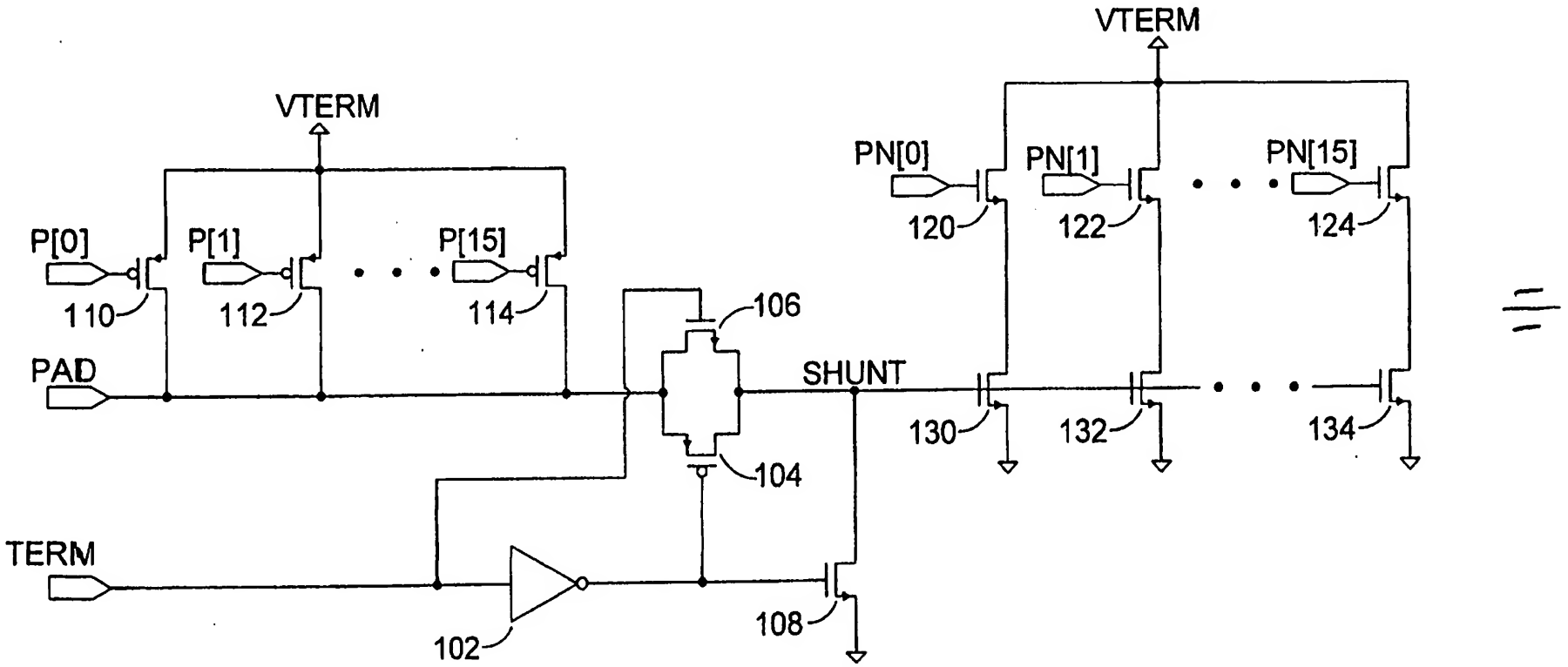
VTERM
VTERM
P[0]
P[1]
P[15]
110
112
114
PAD
106
104
SHUNT
PN[0]
PN[1]
PN[15]
120
122
124
130
132
134
TERM
102
108

FIG. 1

REDUCED CURRENT VARIABILITY I/O BUS TERMINATION

FIELD OF THE INVENTION

[0001] The present invention relates generally to integrated circuits, and more particularly, to techniques and circuits for improving noise margins on on-chip terminated I/O busses and reducing power supply droop and ground bounce oscillations.

BACKGROUND OF THE INVENTION

[0002] One of the causes of reduced, or variable, termination voltages is a change in the amount of current drawn from the termination voltage supply lines. The changes in the amount of current drawn excites oscillations in the inherent inductances in the termination voltage lines. These inherent inductances include inductaces from the package leads and bond wires. The frequency of these oscillations depends upon a number of factors that vary from package-to-package and chip-to-chip. However, on a high-performance I/O (input/output) bus, the frequency of operation may be much greater than the frequency of the oscillations on termination voltage lines. Accordingly, it is important that the I/O circuits on these busses be designed to operate over a range of termination voltages.

[0003] If circuits are not designed to operate over a range of termination voltages, the lines on the bus may not meet their switch times or noise margin requirements and the operating frequency of the bus may have to be lowered. Thus, to meet frequency goals, the termination voltage may be increased to obtain minimum acceptable operating conditions. This increased termination voltage increases the integrated circuit's power dissipation. Increased power dissipation can increase the cost of several components of a system including the integrated circuit packaging, heat sink, and the system power supply. Furthermore, increasing the termination voltage tends to decrease the operating lifetime of the part thereby increasing the cost of system maintenance and amortized cost.

[0004] Accordingly, there is a need in the art for an apparatus and method that reduces the changes in the amount of current drawn on a bus termination voltage supply.

SUMMARY OF THE INVENTION

[0005] An embodiment of the invention reduces the changes, or variability, in the amount of current drawn from the termination voltage supply of an I/O bus. This, in turn, reduces the range of voltages over which a termination voltage may vary. It is well adapted for fabrication on integrated circuits and can be particularly effective when used on wide, parallel, high-speed I/O busses.

[0006] Instances of an embodiment of the invention are connected to the wires of an on-chip terminated I/O bus. Each instance monitors the wire that it is connected to. If the wire has been pulled low by any device on the bus, the circuit does nothing. If, however, the wire was not pulled low, then the invention shunts current from the termination voltage supply to ground. The turn on and turn off rates for this current shunt are matched to the ramps of current through the termination resistor of the bus.

This makes the variability in current drawn from the termination voltage supply less data dependent. Making the current drawn from the termination voltage supply less data dependant reduces the magnitude of the inductive oscillations on the termination voltage which reduces the range of termination voltages over which the bus must be designed to operate.

[0007] Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 is a schematic illustration of a termination voltage current shunt.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0009] FIG. 1 is a schematic illustration of a termination voltage current shunt. In FIG.1 p-channel metal-oxide-semiconductor field effect transistors (PFETs) **110, 112, 114** represent sixteen PFETs controlled by signals P[0:15]. The PFETs represented by **110, 112,** and **114** provide a termination resistance between the termination voltage supply, VTERM, and an I/O bus line, PAD. Accordingly, the sources of each of the PFETs represented by **110, 112,** and **114** are connected to VTERM and the drains of each of the PFETs represented by **110, 112, 114** are connected to PAD.

[0010] The signals P[0:15] are set by other circuitry such that the resistance collectively provided by the PFETs between VTERM and PAD is roughly constant over a range of variations in the impedance of each individual PFET caused by variations due to manufacturing processes, variations in operating voltage, and temperature effects. The variations in the impedance of these PFETs are often called PVT variations. PVT stands for process, voltage, temperature.

[0011] Similarly, n-channel metal-oxide-semiconductor field effect transistors (NFETs) **120, 122, 124** represent sixteen NFETs controlled by signals PN[0:15]. The signals PN[0:15] are set by other circuitry such that the resistance collectively provided by all of the NFETs represented by **120, 122, 124**, if they were placed in parallel with each other, would be constant over a range of PVT effects. The drain of each of the NFETs represented by **120, 122** and **124** are connected to VTERM. The sources of each of the NFETs represented by **120, 122** and **124** are each connected to the drain of sixteen other NFETs represented by NFETs **130, 132,** and **134**, respectively. The sources of each of the NFETs represented by **130, 132,** and **134** are connected to ground. The gates of each of the NFETs represented by **130, 132,** and **134** are connected to the signal SHUNT.

[0012] In the preferred embodiment, signals P[0:15] and PN[0:15] are set to the same values by connecting P[0] to PN[0], P[1] to PN[1], etc. This reduces the number of signals that need to be distributed. Also, the amount of circuitry required to generate these signals is reduced.

[0013] Input signal TERM indicates whether the termination voltage current shunt is active. TERM is connected to the input of inverter **102** and the gate of NFET **106**. The output of inverter **102** is connected to the gate of PFET **104** and the gate of NFET **108**. The source of NFET **108** is connected to ground and the drain of NFET **108** is connected to SHUNT. The drain of NFET **106** and the source of PFET **104** are both connected to PAD. The source of NFET **106** and the drain of PFET **104** are both connected to SHUNT.

[0014] When TERM is at a logical "0", current is not shunted from VTERM at any time. When TERM is at a logical "0", NFET **106** is off and the output of inverter **102** is at a logical "1". This turns PFET **104** off and NFET **108** on pulling SHUNT to

a logical "0". This ensures that the NFETs represented by **130, 132,** and **134** are all off preventing any current from being shunted from VTERM through the NFETs represented by **120, 122** and **124.**

[0015] When TERM is at a logical "1", the termination voltage current shunt is active and current may be shunted from VTERM through the NFETs represented by **120, 122** and **124** and through the NFETs represented by **130, 132,** and **134** to ground. When TERM is at a logical "1", then NFET **108** is off and NFET **106** and PFET **104** are both on. This allows the voltage on PAD to control the voltage on SHUNT which, in turn, determines the impedance of the NFETs represented by **130, 132,** and **134.**

[0016] Accordingly, when the voltage level on PAD is near ground, the gates of NFETs represented by **130, 132,** and **134** are also near ground. Therefore, the NFETs represented by **130, 132,** and **134** are all in a high-impedance state that prevents a significant amount of current from flowing from VTERM through the NFETs represented by **120, 122** and **124** and through the NFETs represented by **130, 132,** and **134** to ground.

[0017] When the voltage level on PAD is above the threshold voltage of the NFETs represented by **130, 132,** and **134,** these NFETs begin to conduct. This allows current to be shunted from VTERM through the NFETs represented by **120, 122** and **124** and through the NFETs represented by **130, 132,** and **134** to ground.

[0018] In operation, when VTERM is high, PAD is connected to a line of an I/O bus that is terminated at least by an impedance set by the PFETs represented by **110, 112,** and **114** to VTERM. Other devices, either on or off the same integrated circuit, turn on and pull PAD and the rest of that line to lower voltage levels than VTERM. This lower voltage level signals a first logic state of the bus. This first logic state may indicate either a logical "1" or a logical "0" in a binary system, or at least one of a

number of other states in a system with a greater number than two logic states. When PAD and the rest of the line is pulled to lower, a first current flows from VTERM onto PAD through the PFETs represented by **110, 112, and 114**. When PAD and the rest of the line is not pulled lower, there is no current flowing from VTERM through the PFETs represented by **110, 112, and 114**. Accordingly, without the termination voltage current shunt the amount of current flowing from VTERM may vary considerably—from zero to the first current amount.

[0019] When the termination voltage current shunt is connected and active and PAD is not pulled lower (and hence there is not current flowing through the PFETs represented by **110, 112, and 114**) the NFETs represented by **130, 132, and 134** are turned on causing a second current to flow from VTERM through the NFETs represented by **120, 122** and **124** and through the NFETs represented by **130, 132,** and **134** to ground. When this second current is set to approximate the first current, above, by appropriate sizing of the transistors represented by **120, 122, 124 130, 132,** and **134** and the state of PN[0:15], the variability in the amount of current drawn from VTERM that depends upon the voltage level of PAD is reduced.

[0020] Although a specific embodiment of the invention has been described and illustrated, the invention is not to be limited to the specific forms or arrangements of parts so described and illustrated. The invention is limited only by the claims.

CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a termination voltage supply; and,

an I/O bus signal wherein a shunt (130, 132, 134) draws current from said termination voltage supply when said I/O bus signal is above a threshold voltage.

2. The integrated circuit of claim 1 wherein said current is a first current and said first current approximates a second current wherein said second current is an amount of current drawn from said termination voltage supply when said I/O bus signal is at a low voltage level.

3. The integrated circuit of claim 2 wherein said first current approximates said second current in timing and magnitude.

4. A method of reducing the variability in current drawn from a termination voltage supply, comprising:

drawing a first current from said termination voltage supply that approximates a second current wherein said second current is an amount of current drawn from said termination voltage supply when a controlled impedance voltage terminated I/O bus signal is in a first state.

5. The method of claim 4 wherein said first current approximates said second current in timing and magnitude as said I/O bus signal switches to said first state.

6. The method of claim 4 wherein said first current approximates said second current in timing and magnitude as said I/O bus signal switches from said first state.

7. An integrated circuit, comprising:

a voltage terminated I/O bus signal that is terminated to a termination voltage supply through a controlled impedance (110, 112, 114) ;

a shunt (130, 132, 134);

a shunt control circuit (102, 104, 106, 108) that turns on said shunt (130, 132, 134) when said I/O bus signal is at a first threshold voltage.

8. The integrated circuit of claim 7 wherein said shunt control circuit (102, 104, 106, 108) uses the intrinsic threshold voltage of a field-effect transistor (130, 132, 134) to set said first threshold voltage.

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Application No: GB 0200033.9 **Examiner:** Keith Sylvan
Claims searched: 1-8 **Date of search:** 24 July 2002

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): H3P (PDM,PHFD,PHFN,PHX) H4P (PPC)

Int Cl (Ed.7): H03K (19/003,19/0175,19/018,19/0185) H04L (25/02,25/08) G06F (13/40)

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A,E	GB2368475 A	HP. See the abstract.	-
A	US6127839	Micron. See the abstract.	-
X	US5304856	AT&T. See figures 2 or 3.	4-6

9

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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